Welcome to the Cadence design tool pages of the Department of Electrical and Computer Engineering at State University of New York at Binghamton. This page contains information about the courses and research projects that make use of the Cadence design tools. Students and faculty of the Department of Electrical and Computer Engineering use Cadence tools extensively for both education and research purposes.

Research Projects:

- **PUF Design in Dark Silicon** (Prof. Aaron Carpenter):
  
  Design physical unclonable function circuits to provide hardware-based secret keys. The analysis requires circuit schematics, timing analysis, and possibly layout-level design to determine sizes, variation, timing, and power. Layout- and circuit-level analyses are required to fully understand the on-chip behavior of these devices.

- **Low-Power Circuit Design in High Variation Chips** (Prof. Aaron Carpenter):
  
  At ever smaller transistor sizes, variation increases to become a significant factor in the timing and power of CMOS chips. This project explores alternatives to conventional CMOS circuits, such as domino logic or DCVSL, with the intent of finding pockets of superiority for replacing CMOS in near-threshold computing in the high-variation chip.

Courses:

- **EECE 455/574: CMOS VLSI Circuits and Architectures** (Prof. Zhanpeng Jin):
  
  This course will provide an overview of the MOS transistor, circuit characterization and performance estimation. Specifically, the course covers CMOS layout design rules, CMOS logic families, basic cell designs (gates, latches, memory cells, etc.), floor planning. Project involves use of Cadence design tools to design a small chip (such as a small CPU, associative memory, array multiplier) that will eventually be fabricated using the MOSIS facilities.

- **EECE 575: VLSI System Design** (Prof. Zhanpeng Jin):
Advanced issues in VLSI microprocessor design: datapath and control design techniques and tradeoffs, using cell libraries of datapath components. Team project involves the specification, design, and implementation of a (pipeline) RISC CPU that will eventually be fabricated using the MOSIS facilities.

All courses require advanced design projects. For VLSI courses usage of Cadence Design tools is required. For EECE 455/574, students can use Cadence design tools to extract transistor parameters for performance analysis in HSPICE. Cadence is also used by our colleagues in the Department of Computer Science in courses such as CS 514, CS 515, CS 520.

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